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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,578	07/29/2003	Antoni Fertner	1410-794	4094

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2128	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,578	FERTNER ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,15-27 and 35-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,15-27 and 35-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *May and Sept., 05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on 09/06/2005. Claims 8-14 and 28-34 are cancelled. Claims 1-7, 15-27, and 35-40 are pending in the action.

Drawings

The drawings filed on 07/29/2003 are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1- 7, 15-27, and 35-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gopal, US patent no. 6,134,513 in view of Mabuchi et al, US patent no. 6,871,334 B2.

As per claim 1, Gopal discloses a method and system including computer program product for simulating a large, hierarchical resistive network with feature limitations very similar to the claimed invention. According to Gopal, the method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

Arranging the system equations for solving the device characteristics,

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10). Gopal does not expressly disclose a step "partitioning the admittance matrix and generating a simplified equation system based on the partitioning of step". Such feature is however well-known in the art. In fact, Mabuchi teaches a method of solving a system equation of admittance matrixes by partitioning the admittance matrixes into partitions and generating a simplified system equation based on the partitioning process as claimed (col. 8, lines 39-67, col. 13, lines 5 to col. 14, line 7) to reduce equivalent matrix and simplify the matrix solving (col. 3, lines 40-54).

This would motivate practitioner in the art at the time of the invention was made to combine the teaching of matrix partitioning into the Gopal circuit analysis to reduce memory and processing time in solving the matrix system equation.

As per claims 2-3, Gopal discloses the system is to solve for network transfer function and resistive network components as claimed.

As per claim 4, Gopal discloses the admittance matrix for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 5, Gopal discloses the admittance blocks for the plural subcircuits are parsed or situated on a main diagonal of the admittance matrix (Figs. 15 and 16),

and the admittance matrix is symmetrical (Fig. 16, col. 10, lines 41-68). Mabuchi teaches the step of connecting partitions with different types of connectivity blocks and the connectivity blocks are symmetry as claimed (col. 8, lines 40-54, cols. 9 and 10, for example) to reduce the size and memory, and to improve matrix solving time.

As per claims 6 and 7, Mabuchi teaches partitioning interest circuit nodes for the analysis.

As per claim 15, Gopal discloses a computer program product for simulating a large, hierarchical resistive network with feature limitations very similar to the claimed invention. According to Gopal, program product includes means:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including main circuit admittance blocks for main circuit, sub-circuit admittance blocks for subcircuits, block connectivities, symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

Gopal does not expressly disclose a step "generating and inserting a plural types of connectivity blocks so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix" as claimed. Such feature is however well-known in the art. In fact, Mabuchi teaches a method of solving a system equation of admittance matrixes by partitioning the admittance

matrixes into partitions and generating a simplified system equation based on the partitioning process as claimed (col. 8, lines 39-67, col. 13, lines 5 to col. 14, line 7) to reduce equivalent matrix and simplify the matrix solving (col. 3, lines 40-54), and the step of connecting partitions with different types of connectivity blocks and the connectivity blocks are symmetry as claimed (col. 8, lines 40-54, cols. 9 and 10, for example) to reduce the size and memory, and to improve matrix solving time.

This would motivate practitioner in the art at the time of the invention was made to combine the teaching of matrix partitioning and using the connectivity blocks with different types of symmetric connectivity blocks into the Gopal circuit analysis to reduce memory and processing time in solving the matrix system equation.

As per claims 16-17, Gopal and Mabuchi disclose the system is to solve for network transfer function such as node voltage or node currents, subcircuit blocks and resistive network components as claimed.

As per claims 18 and 19, Gopal discloses the network transfer function, node voltage, node current, etc. for a plurality of circuit components or subcircuits (Figs. 15). Mabuchi teaches connectivity blocks on opposite sides of the main diagonal (symmetric) of the admittance matrix to reduce matrix computation and memory requirement (col. 3, lines 40-54).

As per claim 20, Gopal discloses the admittance blocks for the plural subcircuits such as filter, circuit transformers, etc. as claimed (Figs. 15 and 16), and the admittance matrix is symmetrical (Figs. 5, 16, col. 5, lines 56-65, col. 10, lines 41-68).

As per claim 21, Gopal discloses a method and system including computer program product for simulating a large, hierarchical resistive network with feature limitations very similar to the claimed invention. According to Gopal, the method includes:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

Arranging the system equations for solving the device characteristics,

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10). Gopal does not expressly disclose a step "partitioning the admittance matrix and generating a simplified equation system based on the partitioning of step". Such feature is however well-known in the art. In fact, Mabuchi teaches a method of solving a system equation of admittance matrixes by partitioning the admittance matrixes into partitions and generating a simplified system equation based on the partitioning process as claimed (col. 8, lines 39-67, col. 13, lines 5 to col. 14, line 7) to reduce equivalent matrix and simplify the matrix solving (col. 3, lines 40-54).

This would motivate practitioner in the art at the time of the invention was made to combine the teaching of matrix partitioning into the Gopal circuit analysis to reduce memory and processing time in solving the matrix system equation.

As per claims 22-23, Gopal discloses the system is to solve for network transfer function and resistive network components as claimed.

As per claim 24, Gopal discloses the admittance matrix for a plurality of circuit components or subcircuits (Figs. 15).

As per claim 25, Gopal discloses the admittance blocks for the plural subcircuits are parsed or situated on a main diagonal of the admittance matrix (Gopal, Figs. 15 and 16), and the admittance matrix is symmetrical (Gopal, Fig. 16, col. 10, lines 41-68). Mabuchi teaches the step of connecting partitions with different types of connectivity blocks and the connectivity blocks are symmetry as claimed (col. 8, lines 40-54, cols. 9 and 10, for example) to reduce the size and memory, and to improve matrix solving time.

As per claims 26-27, Gopal discloses circuit cut node analysis with limitations of nodal analysis, node rearrangement, simplifying node equations, node equations, node transfer functions, etc. as claimed.

As per claim 35, Gopal discloses a computer program product for simulating a large, hierarchical resistive network with feature limitations very similar to the claimed invention. According to Gopal, program product includes means:

Generating an admittance matrix for an electrical which is being analyzed, the admittance matrix including main circuit admittance blocks for main circuit, subcircuit admittance blocks for subcircuits, block connectivities, symbolic expressions for at least some circuit components of the electric circuit (col. 5, lines 55-65, col. 9, line 50 to col. 10, line 40),

And linearly and algebraically solving an equation system including the admittance matrix for analyzing at least a part of the electric circuit (Figs. 15 and 16, cols. 9 and 10).

Gopal does not expressly disclose a step "generating and inserting a plural types of connectivity blocks so that differing types of connectivity blocks are symmetric with respect to one another across the main diagonal of the admittance matrix" as claimed. Such feature is however well-known in the art. In fact, Mabuchi teaches a method of solving a system equation of admittance matrixes by partitioning the admittance matrixes into partitions and generating a simplified system equation based on the partitioning process as claimed (col. 8, lines 39-67, col. 13, lines 5 to col. 14, line 7) to reduce equivalent matrix and simplify the matrix solving (col. 3, lines 40-54), and the step of connecting partitions with different types of connectivity blocks and the connectivity blocks are symmetry as claimed (col. 8, lines 40-54, cols. 9 and 10, for example) to reduce the size and memory, and to improve matrix solving time.

This would motivate practitioner in the art at the time of the invention was made to combine the teaching of matrix partitioning and using the connectivity blocks with different types of symmetric connectivity blocks into the Gopal circuit analysis to reduce memory and processing time in solving the matrix system equation.

As per claims 36-37, Gopal discloses the system is to solve for network transfer function such as node voltage or node currents, and resistive network components as claimed. Mabuchi teaches the step of connecting partitions with different types of connectivity blocks and the connectivity blocks are symmetry as claimed (col. 8, lines

40-54, cols. 9 and 10, for example) to reduce the size and memory, and to improve matrix solving time.

As per claims 38 and 39, Gopal discloses the network transfer function, node voltage, node current, etc. for a plurality of circuit components or subcircuits (Figs. 15). Mabuchi teaches the step of connecting partitions with different types of connectivity blocks and the connectivity blocks are symmetry as claimed (col. 8, lines 40-54, cols. 9 and 10, for example) to reduce the size and memory, and to improve matrix solving time.

As per claim 40, Gopal discloses the admittance blocks for the plural subcircuits such as filter, circuit transformers, etc. as claimed (Figs. 15 and 16), and the admittance matrix is symmetrical (Figs. 5, 16, col. 5, lines 56-65, col. 10, lines 41-68).

Response to Arguments

Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent no. 6,577,992, issued to Tcherniaev et al, on June 2003

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Q. Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nov. 19, 2005

Thai Phan
Patent Examiner